What is claimed is:

1. A frequency divider comprising:

a first divider configured to divide an input signal, and to generate a first high-frequency signal;

a second divider configured to divide a second high-frequency signal, and to generate an output signal;

a third divider configured to generate a third high-frequency signal; and

a mixer configured to execute arithmetic processing for the first and third high-frequency signals, and to generate the second high-frequency signal.

2. The frequency divider of claim 1, wherein the third divider divides the output signal and generates the third high frequency signal.

3. The frequency divider of claim 2, wherein the mixer executes subtraction processing as the arithmetic processing for the first high-frequency signal and the third high-frequency signal.

4. The frequency divider of claim 2, wherein the mixer executes subtraction processing or addition processing as the arithmetic processing for the first high-frequency signal and the third high-frequency signal.

5. The frequency divider of claim 2, wherein the first, second, and third dividers respectively comprise a plurality of stages of cascade-connected first 1/2 dividers, second 1/2 dividers, and third 1/2 dividers.

6. The frequency divider of claim 5, wherein a switch signal stopping operation of the third divider is supplied to the third 1/2 divider.

7. The frequency divider of claim 2, wherein division ratios of the second divider and the third divider are variable.

8. The frequency divider of claim 2, further comprising a filter connected between the third divider and the mixer.

9. The frequency divider of claim 2, further comprising a switch circuit connected between the third divider and the mixer.

10. The frequency divider of claim 2, further comprising a switch circuit connected between the second divider and the third divider.

11. The frequency divider of claim 1, wherein the third divider divides an external reference clock, and generates the third high frequency signal.

12. The frequency divider of claim 11, wherein the first, second, and third dividers respectively comprise a plurality of stages of cascade-connected first 1/2 dividers, second 1/2 dividers, and third 1/2 dividers.

13. The frequency divider of claim 11, wherein the mixer executes subtraction processing or addition processing as the arithmetic processing for the first high-frequency signal and the third high-frequency signal.

14. The frequency divider of claim 11, wherein division ratios of the second divider and the third divider are variable.

15. The frequency divider of claim 11, wherein the third divider further generates a fourth high-frequency signal.

16. The frequency divider of claim 15, further comprising a first output mixer configured to execute arithmetic processing for the output signal and the fourth high-frequency signal.

17. A semiconductor integrated circuit comprising:

a first divider integrated on a semiconductor chip and configured to divide an input signal, and to generate a first high-frequency signal;

a second divider integrated on the semiconductor chip and configured to divide a second high-frequency signal, and to generate an output signal;

a third divider integrated on the semiconductor chip and configured to generate a third high-frequency signal; and

a mixer integrated on the semiconductor chip and configured to execute arithmetic processing for the first and third high-frequency signals, and to generate the second high-frequency signal.

18. A phase locked loop circuit comprising:

a comparison oscillator configured to generate an oscillation signal having a frequency corresponding to a phase difference between a reference clock and a

comparison clock; and

a frequency divider configured to divide the oscillation signal to generate a first high-frequency signal, and to divide a second high-frequency signal, and to generate a third high-frequency signal, and to execute arithmetic processing for the first and third high-frequency signals and to generate the second high-frequency signal.

19. The phase locked loop circuit of claim 18, wherein the frequency divider comprises:

a first divider configured to generate the first high-frequency signal;

a second divider configured to divide the second high-frequency signal, and to generate an output signal;

a third divider configured to divide the output signal, and to generate the third high-frequency signal; and

a mixer configured to generate the second high-frequency signal.

20. The phase locked loop circuit of claim 18, wherein the frequency divider comprises:

a first divider configured to generate the first high-frequency signal;

a second divider configured to divide the second high-frequency signal, and to generate an output signal;

a third divider configured to divide the reference clock, and to generate the third high-frequency signal; and

a mixer configured to generate the second high-frequency signal.